

PATENT APPLICATION
Docket N . 9903-071
Client No. S02US035




Applicant: Jin-Hyuk LEE, Gu-Sung KIM, Dong-Ho LEE and Dong-Hyeon JANG
Serial No: not yet assigned Examiner: not yet assigned
Filing Date: October 21, 2003 Group: not yet assigned
Title: METHOD FOR MANUFACTURING A WAFER LEVEL CHIP SCALE PACKAGE

INFORMATION DISCLOSURE CITATION
FORM PTO-1449 (Modified)




U.S. PATENT DOCUMENTS

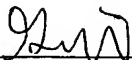
<u>Exam</u> <u>Init</u>	<u>Ref</u>	<u>Document</u> <u>Number</u>	<u>Issue</u> <u>Date</u>	<u>Name</u>	<u>Class</u>	<u>Sub</u> <u>Class</u>
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FOREIGN PATENT DOCUMENTS

<u>Exam</u> <u>Init</u>	<u>Ref</u>	<u>Document</u> <u>Number</u>	<u>Publication</u> <u>Date</u>	<u>Country</u>	<u>Name</u>
	_____	2001-04529	1/15/2001	Korea	Sun-Jin Cho
	_____	2000-65487	11/15/2000	Korea	Lee and Sim
	_____	2000-286283	10/13/2000	Japan	Kuniyasu

OTHER DOCUMENTS

<u>Exam</u> <u>Init</u>	<u>Ref</u>	<u>Author, Title, Date, Pertinent Pages, Etc.)</u>
	_____	English language of Korean Abstract for Korean Patent Publication No. 2001-04529, filed 1/15/2001.
	_____	English language of Korean Abstract for Korean Patent Publication No. 2000-65487, filed 11/15/2000.
	_____	English language of Japanese Abstract for Japanese Patent Publication No. 2000-286283, filed 10/13/2000.

Examiner: 

Date Considered: 6-7-5